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CHIP SCALE PACKAGE AND METHOD FOR MARKING THE SAME

A chip scale package includes a plurality of terminals for making external electrical connections and a chip. The chip has a plurality of bonding pads on an active surface thereof, and the bonding pads of the chip are electrically connected to the terminals. The backside surface of the chip is exposed from a surface of the package. The present invention is characterized by having an ink mark on the backside surface of the chip. The present invention further provides a method for making the chip scale package at the wafer level.